
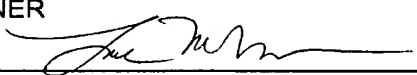


FORM PTO-1449 (SUBSTITUTE)  U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE  INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))				Attorney Docket No.: M&N-IT255 Appl. No.  Applicant KARL SCHROEDINGER ET AL.  Filing Date November 16, 2001 Group Art Unit <u>2816</u>			
1c857 U.S. PTO 09/992281 							
EXAMINER INITIALS	A	PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
<u>LM</u>	A	5,015,872	05/91	Rein	327	231	
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						
FOREIGN PATENT DOCUMENT							
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES   NO
	J						
	K						
	L						
	M						
	N						
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)							
<u>LM</u>		Thomas H. Lee et al.: "A 2.5 V CMOS Delay-Locked Loop for an 18 Mbit, 500 Megabyte/s DRAM", IEEE Journal of Solid-State Circuits, Vol. 29, No. 12, December 1994, pp. 1491-1496;					
EXAMINER				DATE CONSIDERED			
				<u>01/24/2003</u>			
EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							